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322352(28)

B. E. (Third Semester) Examination, April-May 2020

(New Scheme)

(CSE Branch)

BASIC ELECTRONICS

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

***Note** : Part (a) of each question is compulsory. Attempt any **one** from (b) and (c). Part (a) = 2 marks, (b) and (c) = 14 marks. Assume suitable data if any.*

Unit-I

1. (a) What is the effect of temperature on V-I characteristics of diode? 2

   (b) (i) What is the need for biasing? Explain the forward and reverse biasing of diode. 7

   (ii) Derive the equation of transition capacitance of P-N junction diode. 7

Or

(c) (i) The resistivity of the two sides of silicon step junction are $P_p = 10\ \Omega$-cm and $P_p = 3{\cdot}5\ \Omega$-cm. Calculate the height of the potential barrier. Assume $\mu_n = 1500\ cm^2/V\text{-}s$, $\mu_p = 475\ cm^2/V\text{-}s$ $n_i = 1{\cdot}45 \times 10^{10}\ cm^3$. 7

(ii) Determine the concentration of free electrons and goles in a sample of germanium at 300°K which has a concentration of donor atoms equal to 2×10^{14} atoms/cm^3 and a concentration of acceptor atoms equal to 3×10^4 atoms/cm^3. Is this *p* or *n* type germanium. 7

Unit-II

2. (a) What is ripple factor in rectifier? 2

(b) (i) Why bridge rectifier is preferred over center tapped rectifier? Derive the equation for efficiency, transfer utilization factor and voltage regulation for bridge rectifier. 7

(ii) What is zener break down mechanism? Why zener diode is used as voltage regulator? Explain. 7

Or

(c) (i) A full wave bridge rectifier circuit uses two silicon diodes with a forward resistance of 20 Ω each. Voltmerter connected across the load of 1 kΩ read 55·4 V.

Calculate :

1. RMS current
2. Average voltage
3. Ripple factor
4. T.U.F. 7

(ii) For the voltage regulation circuit find the minimum and maximum zener current if source voltage varying from (80-120 V). Source resistance is 5 kΩ, load resistance is 10 kΩ, and voltage across the zener is 50 V. 7

Unit-III

3. (a) Which configuration of transistor is known as voltage follower configuration and why? 2

(b) (i) What is early effect? Also explain the consequences of base width modulation. 7

(ii) Draw and explain the input and output characteristics of common emitter configuration of transistor. 7

Or

(c) (i) Explain the operation of transistor of an amplifier. 7

(ii) For a certain transistor, $I_C = 5.255$ mA, $I_B = 100$ μA and $F_{CBO} = 5$ μA.

1. Calculate α, β and I_E.

2. Determine the new level of I_B required to make IC = 15 mA. 7

Unit-IV

4. (a) What is the need for biasing? 2

(b) (i) Derive the stability factor '*S*' for voltage divider bias circuit. 7

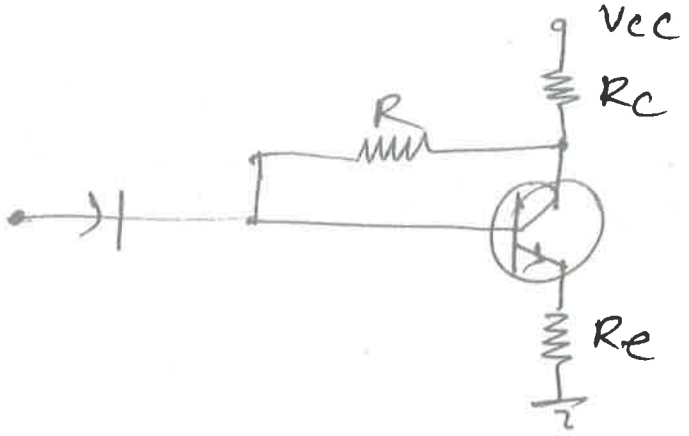
(ii) What is thermal runaway? Derive the equation for thermal stability of the transistor. 7

Or

(c) (i) Explain the method of diode compensation. 7

(ii) In the circuit shown, $V_{CC} = 24$ V, $R_C = 10$ K and $R_e = 270\ \Omega$. If a silicon transistor is used with $\beta = 45$ and if under quiscent conditions $V_{CE} = 5$ V, determine :

1. R
2. the stability factors. 7



Unit-V

5. (a) Give any two difference between FET and BJT. 2

(b) (i) Explain the basic operation for N-channel JFET with proper diagram. 7

(ii) Draw and explain the drain characteristics of N-channel TFET and explain all the regions. 7

Or

(c) (i) Explain the enhancement mode P type with proper diagram. 7

(ii) Write down five differences between JFET and MOSFET. 7